计组期末复习

概念选择判断题

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2022-2023
1. What is the range of exponent of IEEE 754 single precision? ( )
A. 1~254
B. -128~126
C. -126~127
D. -127~128

2.The SRAMs are basically used as _______ ( )
A. register
B. cache
C. main memory
D. disk

4. Consider the following C code:
typedef unsigned char *pointer; // sizeof(unsigned char) = 1 byte
void show_bytes(pointer start, size_t len) {
for (int i = 0; i < len; i++)
printf("0x%x\n", start[i]);
}
int main() {
int a = 0x11223344;
show_bytes((pointer) &a, sizeof(int));
}
If this C code runs on a little-endian machine, what will we get on the third
line of the
terminal output? ()
A. 0x11
B. 0x22
C. 0x33
D. 0x44

5. The reason for the implementation of the cache memory is _____. ()
A. to increase the internal memory of the system
B. the difference in speeds of operation of the processor and memory
C. to reduce the memory access time
D. all of the mentioned

6. Which of the following allows simultaneous write and read operations?
A. ROM
B. EROM
C. RAM
D. None of the above

7. The copy-back protocol is used _______. ()
A. to copy the contents of the memory onto the cache
B. to update the contents of the memory from the cache
C. to remove the contents of the cache and push it on to the memory
D. none of the mentioned
```

9. The function of assembler is _____. ()
A. Transforming high level language to binary language
B. Transforming binary language to high level language
C. Transforming assembly language to machine code
D. Transforming high level language to assembly language

10. The temporal aspect of the locality of reference means (_____).
A. That the recently executed instruction won't be executed soon
B. That the recently executed instruction is temporarily not referenced
C. That the recently executed instruction will be executed soon again
D. None of the mentioned

12. Given the following RISC-V assembly code (and assuming all registers start at 0):
addi t1, x0, 10
add t2, t1, t1
repeat: addi t2, t2, -4
add t3, t2, t2
addi t1, t1, -2
bne x0, t1, repeat
What is the final value of register t3?
A.0
B.-4
C.8
D.4

13. A multilevel page table is preferred in comparison to a single level page table for
translating virtual address to physical address because_____()
A. it reduces the memory access time to read or write a memory location
B. it helps to reduce the size of page table needed to implement the virtual address space
of a process
C. it is required by the translation lookaside buffer
D. it helps to reduce the number of page faults in page replacement algorithms

15. Which one is not one of the five classic components of a computer?
A. Input
B. Bus
C. Memory
D. Output

18. Assume a 5-stage pipelined RISC-V CPU with no forwarding. How many stalls would there need to be in order to fix all data hazards (assuming that we can read and
write to the RegFile on the same cycle)?
sub t1, s0, s1
or s0, t0, t1
sw s1, 100(s0)
add s2, s0, s2
lw t1, 104(s0)
A. 2
B. 3
C. 4

D. 5

19. The bit width of PC is determined by ( ).
A. Memory word length
B. Memory capacity
C. Instruction word length
D. Bit width of general-purpose registers

20. The fastest data access is provided using (_____).
A. Caches
B. DRAM's
C. SRAM's
D. Registers

II. TRUE OR FALSE (10 points)
1. ____ The LRU can be improved by providing a little randomness in the access.
2. ____ The associative mapping is costlier than direct mapping.
3. ____ In the memory hierarchy, as the speed of operation increases the memory size
also increases.
4. ____ The pipeline bubbling is a method used to prevent data hazard and control
hazards.
5. ____ Virtual memory allows a single program to expand its address space beyond the limits of main memory.
6. ____ Cache block size (B) can affect both miss rate and miss latency.
7. ____ There is no way to reduce compulsory misses.
8. ____The CPI of superscalar processors can be less than one.
9. ____The higher the memory bandwidth, the larger the cache block.
10. ____The page table is stored in the disk.

2021-2022
1. With the help of _____ we reduce the memory access time. (_____)
A. SDRAM
B. Cache
C. Heaps
D. Higher capacity RAMs

4. A processor performing fetch or decoding of different instruction during the execution of another
instruction is called (_____).
A. Super-scaling
B. Pipe-lining
C. SIMD
D. MIMD

5. In memory-mapped I/O (_____).
A. The I/O devices and the memory share the same address space
B. The I/O devices have a separate address space
C. The memory and I/O devices have an associated address space
D. A part of the memory is specifically set aside for the I/O operation

6. The spatial locality of reference means (_____).
A. That the recently referenced memory location is referenced again next
B. That the recently referenced won't be referenced again
C. That the memory location referenced will be referenced at a later time
D. That the locations in nearby addresses of the memory location referenced will be referenced soon

8. When silicon chips are fabricated, a very common defect is for one signal wire to get "broken"
and always register a logical 0. This is often called a "stuck-at-0" fault. Which instruction below
operates correctly if the RegWrite wire is stuck at 0? (_____)
A. auipc
B. jal
C. addi
D. sw

10. What is used to compute the offset of all branch instructions? (_____)
A. Compiler
B. Assembler
C. Linker
D. Loader

12. The stalling of the processor due to the unavailability of the instructions is called as (_____).
A. Control hazard
B. Structural hazard
C. Data hazard
D. Input hazard

14. In _____ protocol the data is directly written into the main memory. (_____)
A. Write through
B. Write back
C. Write first
D. Write allocate

15. Consider a normal 5-stage pipeline. If a unit in the pipeline completes its task before the time
period, then (_____).
A. It will perform some other task in the remaining time
B. Its time gets reallocated to a different task
C. It will remain idle for the remaining time
D. None of the above

1. _ _The assembler produces an executable.
2. _ _Two's complement in 8 bits for -127 is 1000 0000.
3. _ _The penalty for a page fault is about the same as the penalty for a cache miss.
4. _ _A linear page table takes up more memory as the process uses more memory.
5. _ _The page table is stored in main memory.
6. _ _Large block size of a cache may increase the average access time or the miss rate.
7. _ _Capacity misses would not occur under perfect replacement policy.
8. _ _Choice of hardware and software parallelism is independent.

9. _ _A branch target buffer in the IF stage can cache the branch results that tell whether the branch
was taken the last time it was execute.
10. _ _Superscalar processors use multiple execution units for additional instruction level
parallelism.

2020-2021
3. _____ is generally used to increase the apparent size of physical memory.
A. Secondary memory B. Virtual memory C. Hard disk D. Disks

4. The time delay between two successive initiations of memory operation is _____.
A. Memory access time B. Memory search time
C. Memory cycle time D. Instruction delay

5. When performing a looping operation, the instruction gets stored in the _____.
A. Registers B. Cache C. System heap D. System stack

6. The instruction “lw x5, 40(x6)” does _____.
A. Loads the value of x5 and stores it x6
B. Loads the value of x5 and stores it in Memory[x6 + 40]
C. Loads the value in Memory[x6 + 40] and stores it in x5
D. Loads the value of x6 and stores it in Memory[x5 + 40]

7. The addressing mode which makes use of both register file and memory is _____.
A. Immediate addressing B. Register addressing
C. Base addressing D. PC-relative addressing

8. In a system which has 64 registers, the register id is _____ long.
A. 32-bit B. 8-bit C. 5-bit D. 6-bit

9. The processor keeps track of the result of its operations using flags called _____.
A. Conditional code flags B. Test output flags
C. Type flags D. None of the mentioned

10. The wrong statement/s regarding interrupts and subroutines among the following is/are _____.
i) The subroutine and interrupts have a return statement
ii) Both of them alter the content of the PC
iii) Both are software oriented
iv) Both can be initiated by the user
A. i, ii, and iv B. ii and iii
C. iv D. iii and iv

11. The execution of the following two instructions may have the _____.
ld x5,0(x6)
sd x5,0(x6)
A. RAW (Read after Write) B. WAW (Write after Write)
C. WAR (Write after Read) D. No data dependency

14. Which of the following cache designer guideline is not valid?

A. Fully associative caches have no conflict misses.
B. In reducing misses, associativity is more important than capacity.
C. The higher the memory bandwidth, the larger the cache block.
D. The shorter the memory latency, the smaller the cache block.

1. The miss penalty can be reduced by improving the mechanisms for data transfer between the
different levels of hierarchy.
2. For forwarding you need only look at the data available in the WB stage.
3. In a system where multiple programs are running, the physical address space must be larger
than the total size of the virtual address spaces.
4. In set associative and associative mapping there exists less flexibility.
5. When using the Big Endian assignment to store a number, the sign bits of the number is stored
in the lower order byte of the word.
6. The order in which the return addresses are generated and used is First-In-First-Out.
7. Cache performance is of less importance in faster processors because the processor speed
compensates for the high memory access time.
8. Pipelining improves performance by increasing instruction throughput.
9. A write-through cache typically requires more bus bandwidth than a write-back cache.
10. An executable binary file that can run on a RISC-V CPU may not be able to execute on
another RISC-V CPU.

2019-2020
2. What is the content of stack pointer (SP)? (_____)
A. address of the current instruction
B. address of the next instruction
C. address of the top element of the stack
D. size of the stack

3. What is the function of the compiler? (_____)
A. Translates assembly language into binary instructions.
B. Translates source code into intermediates and immediately executes it.
C. Combines independent programs and resolves labels into an executable file.
D. Translate a high-level language into assembly language.

4. The bit used to signify that the cache location is updated is (_____).
A. Dirty bit
B. Update bit
C. Reference bit
D. Flag bit

5. Interrupts can be generated in response to (_____).
A. detected program errors such as arithmetic overflow or division by zero
B. detected hardware faults
C. input/output activities
D. All of the above.

6. Write Through technique is used in which memory for updating the data? (_____)
A. Virtual memory
B. Main memory
C. Auxiliary memory
D. Cache memory

7. The execution of the following two instructions may have the (_____).
lw x5,0(x6)
lw x7,0(x5)
A. RAW (Read after Write)
B. WAW (Write after Write)
C. WAR (Write after Read)
D. No data dependency.

8. Forwarding is a technique used in a pipeline to reduce the number of stall cycles caused by
hazards. Each sequence of instructions shown below causes a hazard for the version of the
RISC-V pipeline that we studied in class. The pipeline bubble that would be caused by some of
these hazards can be avoided through the use of forwarding. Others cannot. Mark the sequences
for which the bubble cannot be avoided through forwarding. (_____)
A. lw x5, 0(x6)
sll x9, x10, x11
add x7, x8, x5
B. add x7, x8, x9
beq x7, x0, L2
C. sub x5, x6, x7
add x8, x9, x5
D. lw x5, 0(x6)
add x7, x8, x5

9. The RISC-V addressing mode of “jal x1, 100” is (_____).
A. Immediate addressing
B. Base addressing
C. PC-relative addressing
D. None of the above.

10. Which type of parallel computing architecture is no longer commonly encountered in
machines today? (_____)
A. MIMD (Multiple Instruction/Multiple Data Stream)
B. MISD (Multiple Instruction/Single Data Stream)
C. SIMD (Single Instruction/Multiple Data Stream)
D. SISD (Single Instruction/Single Data Stream)

15. The drawback of building a large memory with DRAM (Dynamic Random Access Memory) is
(_____).
A. The large cost factor
B. The inefficient memory organization
C. The Slow speed of operation
D. All of the mentioned

17. What is the RISC-V assembly code for the binary? (_____)
00100100011000111010110000100011
A. sw t1, 600(t2)
B. sw t1, 1200(t2)
C. sw t2, 600(t1)
D. sw t2, 1200(t1)

18. The effectiveness of the cache memory is based on the property of (_____).

A. Locality of reference
B. Memory localization
C. Memory size
D. None of the mentioned

判断题
1. _____Multiple levels of page tables will increase the total amount of page table storage.
2. _____Static RAM is typically used to implement Cache.
3. _____First-level caches are more concerned about miss rate, and second-level caches are more
concerned about hit time.
4. _____Two's complement in 8 bits for -128 is 1000 0000.
5. _____When meeting cache misses, “no write allocate” means only writing to main memory.
6. _____Pipelining a processor implementation probably will increase throughput.
7. _____If hit rates are well below 0.9, then they’re called as speedy computers.
8. _____Assume two cache designs CA and CB have the same block size. CA is a 32 KiB 2-way set
associative cache and CB is a 16 KiB direct-mapped cache. The length of the tag, measured
in the number of bits, is the same in CA and in CB.
9. _____Each stage in pipelining should be completed within 5 cycles.
10. _____If a data cache does not contain a dirty bit, then it must be using a write-through policy.

2018-2019
使用的是MIPS而不是risc-v
1. Which number representation can be used to represents a negative number? (_____)
A. Two’s complement
B. One’s complement
C. Signed magnitude
D. All of above

4. The MIPS addressing mode of “j 254” is (_____).
A. Immediate addressing
B. Pseudodirect addressing
C. PC-relative addressing
D. None of the above.

5. The L1 cache on a high-end processor is most likely to use which technology? (_____)
A. Flash
B. Magnetic disk

C. SRAM
D. DRAM

6. Pipelining a processor implementation probably won't do which of the following: (_____)
A. Decrease latency
B. Increase throughput
C. Allow a faster clock rate
D. All of the above probably will happen

7. What is an advantage of increasing the number of pipelines? (_____)
A. Less complex circuit
B. Faster computation on a whole instruction
C. Faster clock speed
D. Increased clock period

8. The execution of the following two instructions may have the (_____) hazard.
lw R3, 0(R2)
lw R2, 0(R1)
A. RAW (Read after Write)
B. WAW (Write after Write)
C. WAR (Write after Read)
D. No hazards

9. The main purpose of having memory hierarchy is to (_____).
A. Reduce access time
B. Provide large capacity
C. Reduce propagation time
D. Reduce access time & provide large capacity

14. If a system is 64-bit machine, then the length of each word will be (_____).
A. 4 bytes
B. 8 bytes
C. 16 bytes
D. 12 bytes

15. Increasing associativity can reduce (_____).
A. Compulsory misses (cold-start misses)
B. Capacity misses
C. Conflict misses (collision misses)
D. All three misses

16. Which of the following situation will not happen? (_____)
A. TLB (Translation-lookaside Buffer) miss, Cache hit, Page hit
B. TLB miss, Cache miss, Page hit
C. TLB miss, Cache miss, Page miss
D. TLB hit, Cache miss, Page miss

20. The unit which acts as an intermediate agent between memory and backing store to reduce
process time is (_____).
A. TLB's
B. Registers
C. Page tables

D. Cache

判断：
1. ____In 8-bit two's complement numbers, the negative of 10101101 (binary) is 01010011.
2. ____The physical memory is not as large as the address space spanned by the processor.
3. ____Both multithreading and multicore rely on parallelism to get more efficiency from a chip.
4. ____The directly mapped cache no replacement algorithm is required.
5. ____Multiple levels of page tables can also be used to reduce the total amount of page table
storage.
6. ____To help the operating system estimate the LRU pages, some computers provide a dirty bit,
which is set whenever a page is accessed.
7. ____In virtual memory, the number of entries of a page table is equals to the physical page
number.
8. ____The starting address of the page table is stored in TLB.
9. ____Write-through: A scheme that handles writes by updating values only to the block in the
cache, then writing the modified block to the lower level of the hierarchy when the block is
replaced.
10. ___For L2 cache, reducing hit time is as important as reducing miss rate.

2017-2018
1. Which of the following I/O mechanisms requires the least hardware support? ( )
A. Polling B. Interrupt
C. DMA D. None of the above

2. What is the primary characteristic of a CISC architecture? Circle the best answer. ( )
A. Large number of registers
B. Small number of registers
C. Variable length instructions
D. Fixed length instructions

4. A key factor in determining the cost of an integrated circuit is volume. Which of the
following is not reason why a chip made in high volume should cost less? ( )
A. With high volumes, the manufacturing process can be tuned to a particular design,
increasing the yield.
B. It is less work to design a high-volume part than a low-volume part.
C. The masks used to make the chip are expensive, so the cost per chip is lower for higher
volumes.
D. Engineering development costs are high and largely independent of volumes, thus, the
development cost per die is lower with high-volume parts.

5. A group of students were debating the efficiency of the five-stage pipeline when one student
pointed out that not all instructions are active in every stage of the pipeline. After deciding to
ignore the effect of hazards, they made the following four statements. Which one is correct?
( )
A. Allowing jumps, branches, and ALU instructions to take fewer stages than the five required by the load instruction will increase pipeline performance under all
circumstances.
B. Trying to allow some instructions to take fewer cycles does not help, since the
throughput is determined by the clock cycle; the number of pipe stages per instruction affects throughput, not latency.
C. You cannot make ALU instructions take fewer cycles because of the write-back of
the result, but branches and jumps can take fewer cycles, so there is some opportunity for improvement.
D. Instead of trying to make instructions take fewer cycles, we should explore making the pipeline longer, so that instructions take more cycles, but the cycles are shorter. This could improve performance.

6. How the cache conflict misses will be affected by the following modifications? Assume the
baseline cache is set associative. ( )
(a). Double the associativity while keep the capacity and line size constant
(b). Double the number of sets while keep the capacity and line size constant
A. Increase; Decrease B. Decrease; Increase
C. Increase; Increase D. Decrease; Decrease

7. Here is a series of address references given as word addresses: 2, 3, 11, 16, 21, 13, 64, 48, 19,
11, 3, 22, 4, 27, 6, 11. Determine how many misses will happen in each condition.
(a) A direct-mapped cache with 16 one-word blocks that is initially empty. ( )
A. 11 B. 12 C. 13 D. 15
(b) A direct-mapped cache with four-word blocks and a total size of 16 words. ( )
A. 11 B. 12 C. 13 D. 15
(c) A two-way set-associative cache with four-word blocks and a total size of 16 words. Use
LRU replacement. ( )
A. 11 B. 12 C. 13 D. 15

10. If a data cache does not contain a dirty bit, then it must be using a _____ policy. ( )
A. Write through B. Write back
C. Read back D. None of the above

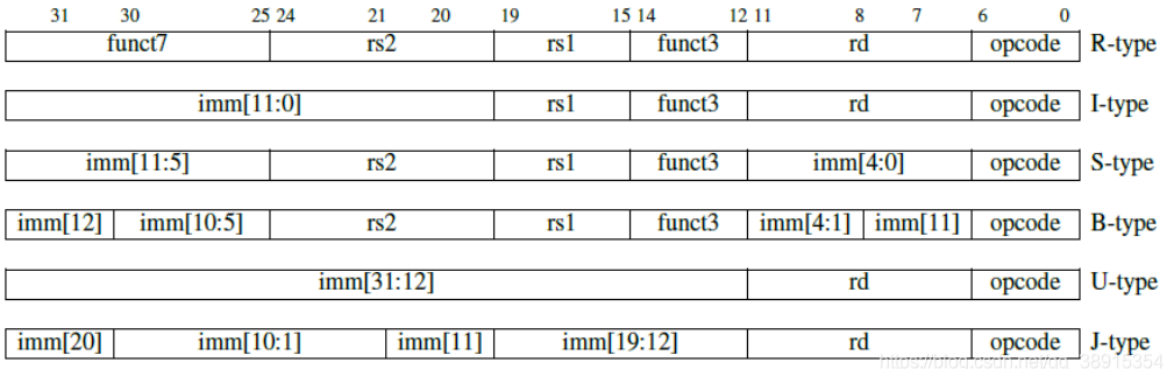
11. Which of the following situation will not happen? ( )
A. TLB miss, Cache hit, Page hit
B. TLB hit, Cache hit, Page miss
C. TLB miss, Cache hit, Page hit
D. TLB hit, Cache hit, Page hit

判断题
1. In the MIPS processor we studied, all instructions were 32-bits wide. ( )
2. MIPS can best be described as a CISC architecture because the instruction set has more than
20 opcodes.（ ）
3. Adding a lower level cache reduces miss penalty. （ ）
4. Increasing set associativity increases hit time. （ ）
5. An instruction takes less time to execute on a pipelined processor than on a nonpipelined
processor (all other aspects of the processors being the same). （ ）
6. A denormalized binary floating point number is any non-zero floating point number that is
not in the form 1.a × 2b, where a and b are integers represented in binary. （ ）
7. The MIPS slt instruction only works correctly if both operand registers contain non-negative
values. （ ）
8. The CPI of superscalar processors can be less than one. （ ）
9. With a 4-entry TLB, 2 physical pages, and 4 virtual pages, the TLB will never be full. （ ）
10. In a function that makes lots of function calls, it is more efficient to save local variables in
temporary registers than in saved registers. （ ）

复习回顾：

概念选择判断题复习：

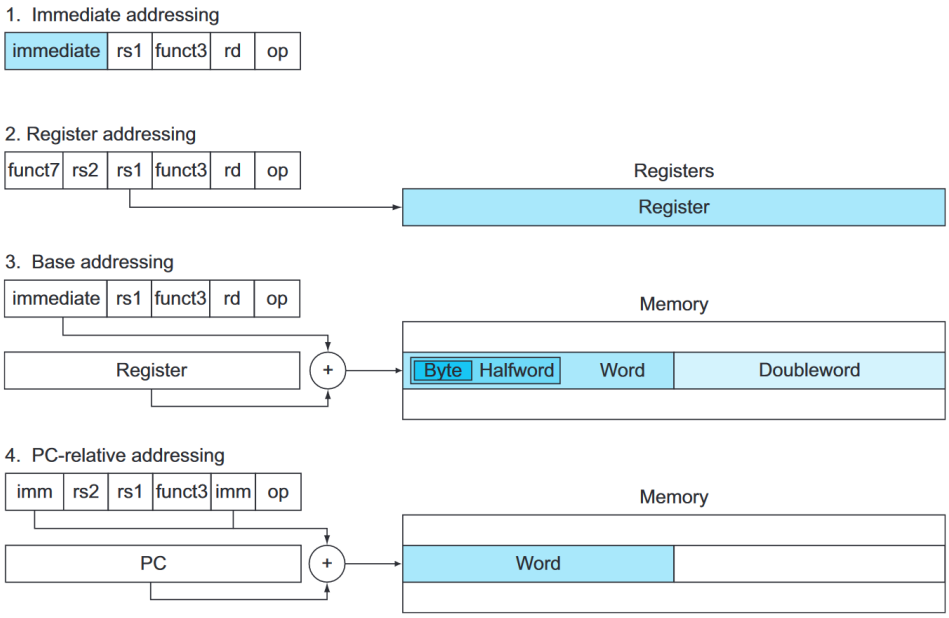
1.机器码对应关系,指令集



2.几种寻址模式的辨析
A. Immediate Addressing（立即数寻址）： 操作数的值直接嵌入在指令中。
addi
B. Register Addressing（寄存器寻址）： 操作数的值存储在寄存器中。
add
C. Base Addressing（基址寻址）： 使用一个基址寄存器加上一个偏移量来计算操作数的地址。
lw

D. PC-relative Addressing（PC相对寻址）： 使用程序计数器（PC）的当前值加上一个偏移量来计算操作数的地址。通常用于实现分支指令。
beq

1. Immediate addressing, where the operand is a constant within the instruction itself.
2. Register addressing, where the operand is a register.
3. Base or displacement addressing, where the operand is at the memory location whose address is the sum of a register and a constant in the instruction.
4. PC-relative addressing, where the branch address is the sum of the PC and a constant in the instruction.



RAW (Read after Write):

含义： 指令 B 试图读取指令 A 刚刚写入的数据。
例子： 如果指令 A 是写入某个寄存器，而指令 B 是读取同一寄存器的值，那么就存在 RAW 依赖。
WAW (Write after Write):

含义： 两个或更多的指令试图在相同的目标写入数据。
例子： 如果有两个指令 A 和 B，它们都试图写入相同的寄存器，那么就存在 WAW 依赖。
WAR (Write after Read):

含义： 指令 B 试图在指令 A 读取数据之后写入相同的位置。
例子： 如果指令 A 是读取某个内存位置，而指令 B 是写入同一内存位置，那么就存在 WAR 依赖。
这些依赖关系是并行计算中的概念，对于多核处理器、超标量处理器等架构的设计和优化非常重要。解决这些依赖性问题可以采用技术如乱序执行、流水线、数据预取等，以提高指令执行的效率。

注意：read和write的对象指的不是memory，而是寄存器

Forwarding is a technique used in a pipeline to reduce the number of stall cycles caused by hazards.
注意指令-ld只有DM之后才可以进行Forward（从内存取数），add则是ALU之后就可以

流水线：

DRAM and SRAM:
SRAM，静态随机存储器（Static Random Access Memory）：

SRAMs are simply integrated circuits that are memory arrays with (usually) a single access port that can provide either a read or a write. SRAMs have a fixed access time to any datum, though the read and write access times may differ(对任何数据都有固定的访问时间，尽管读和写的访问时间可能不同).

SRAMs don't need to refresh and so the access time is very close to the cycle time. SRAMs typically use six to eight transistors per bit to prevent the information from being disturbed when read. SRAM needs only minimal power to retain the charge in standby mode.

- Lower density（密度） (about 1/10 density of DRAM), higher cost

- Static since data is held without refresh if power is on

- Fast access time, often 2 to 10 times faster than DRAM

DRAM ，动态随机存储器（Dynamic Random Access Memory）：

DRAMs use only one transistor per bit of storage, they are much denser and cheaper per bit than SRAM. As DRAMs store the charge on a capacitor, it **cannot be kept indefinitely and must periodically be refreshed**. That is why this memory structure is called dynamic, in contrast to(相反) the static storage in an SRAM cell

DRAMs use a two-level decoding structure, and this allows us to refresh an entire row (which shares a word line) with a read cycle followed immediately by a write cycle.

To improve performance, DRAMs buffer rows for repeated access. The buffer acts like an SRAM; by changing the address, random bits can be accessed in the buffer until the next row access. This capability improves the access time significantly, since the access time to bits in the row is much lower.

- High density, low power, cheap, but slow

- Dynamic since data must be "refreshed" regularly ("leaky buckets")

- Contents are lost when power is lost

注意，SRAM要刷新，DRAM不用刷新。SRAM造价高，更快，常用于cache。DRAM造价低，更慢

写回，写分配：

写直通（write through）：同时写入缓存和内存
通常流量较高，但简化了缓存一致性
写回（write back）：只写入缓存
只有在将条目逐出时才写入内存
每个块可以有一个脏位（dirty bit），进一步减少流量
缓存未命中：

无写分配（no write allocate）：仅写入主存
写分配（write allocate，又称为写取时取回）：将数据读取到缓存
常见组合：
写直通和无写分配
写回和写分配
（另外两种的组合效果较差）

1.写分配（write allocate）是一种缓存管理策略，用于处理写操作时发生的缓存未命中。当发生写操作并且数据不在缓存中时，写分配策略会将相应的数据块从主存（内存）加载到缓存中，然后再执行写操作。这意味着在写操作之前，必须将数据加载到缓存，即使只是为了写入一次。

2.相对应的是"无写分配"策略（no write allocate），当写操作发生缓存未命中时，数据被直接写入主存，而不将其加载到缓存中。这样可以节省一些带宽，但也可能导致对主存的频繁写入，因为数据不会被缓存。

3.在计算机体系结构中，缓存的脏位（dirty bit）是一个标志位，用于指示缓存中的某一块数据是否已被修改（脏）而与主存中的相应数据不一致。脏位通常用于支持写回（write back）缓存策略。
当一个程序对缓存中的数据进行写操作时，如果采用写回策略，该数据会首先被标记为脏，表示与主存中的数据不同步。然后，只有在该缓存块被替换出去（evicted）时，才会将脏数据写回到主存，以确保主存中的数据与缓存中的数据保持一致。
使用脏位的好处在于，它可以减少对主存的写访问次数，从而提高性能。当缓存中的数据被写入但尚未被写回主存时，脏位告诉系统哪些数据需要更新到主存，避免了不必要的主存写入。

中断与轮询：
i) 子程序和中断都有返回语句：这是正确的。子程序调用完成后，通常通过“返回”指令回到调用点。同样，中断处理完成后，系统会通过特殊的返回指令回到中断前的状态。

ii) 它们都会改变程序计数器（PC）的内容：这也是正确的。无论是子程序调用还是中断，都会导致程序计数器指向新的地址（子程序的起始地址或中断处理程序的地址）。

iii) 它们都是软件导向的：这是不正确的。中断既可以是软件导向的（软中断），也可以是硬件导向的（硬中断）。而子程序通常是软件导向的，由程序中的指令明确调用。

iv) 它们都可以由用户发起：这也是不完全正确的。虽然用户可以通过软件来发起子程序调用和软件中断，但硬件中断通常是由硬件事件触发的，而不是直接由用户发起。

状态寄存器：
The processor keeps track of the result of its operations using flags called _____.
A. Conditional code flags B. Test output flags
C. Type flags D. None of the mentioned
avatar
处理器使用名为**A. 条件码标志（Conditional Code Flags）**来跟踪其操作的结果。

条件码标志是处理器状态寄存器的一部分，它们用于指示最近执行的操作的各种条件和结果，例如：

零标志（Zero Flag）：如果操作的结果为零，则设置此标志。
符号标志（Sign Flag）：反映了操作结果的符号（正或负）。
溢出标志（Overflow Flag）：在算术操作导致结果超出其可表示范围时设置。
进位标志（Carry Flag）：在操作导致进位或借位时设置。
这些标志对于控制流指令（如条件跳转指令）非常重要，因为它们根据这些标志的状态来决定程序的执行路径。例如，一个条件跳转指令可能会检查零标志，如果该标志被设置，则跳转到指定的代码部分。

进制转换与浮点数
1. What is the range of exponent of IEEE 754 single precision? ( )
A. 1~254
B. -128~126
C. -126~127
D. -127~128

IEEE 754单精度格式的偏置是127。这意味着指数值以无符号整数的形式存储，实际指数值加上127。8位无符号整数的范围是0到255。减去偏置后得到实际的指数值，范围变为：
最小指数 = 0 - 127 = -127
最大指数 = 255 - 127 = 128
然而，0和255这两个值是为特殊数值（如0、无穷大和NaN）保留的。因此，正常数值的实际指数范围为1到254（经过偏置），对应的实际指数范围是：
最小指数 = 1 - 127 = -126
最大指数 = 254 - 127 = 127
所以，IEEE 754单精度中指数的正确范围是：
-126到127

Two's complement：补码
正数的表示：正数在Two's complement中与其原始的二进制表示相同。例如，如果用8位表示，+5就是00000101。
零的表示：零在Two's complement中只有一种表示，即所有位都是0。例如，用8位表示，0是00000000。
负数的表示：要获取一个负数的Two's complement表示，先找到该数的绝对值的二进制表示，然后将所有位取反（0变为1，1变为0），最后在取反后的数上加1。例如，-5在8位Two's complement中表示为11111011。
范围：在n位Two's complement表示中，可以表示的整数范围是从-2^(n-1)到2^(n-1)-1。例如，8位可以表示的范围是-128到+127。

temporal locality（地点）：The locality principle stating that if **a data location is referenced then it will tend to be referenced again soon**.

spatial locality：The locality principle stating that if **a data location is referenced, data locations with nearby addresses will tend to be referenced soon.**

超标量处理器（superscalar processors）的CPI（每条指令的时钟周期数，Clock Cycles Per Instruction）可以小于一。这是因为超标量处理器能够在一个时钟周期内同时发射和执行多条指令。
在传统的标量处理器中，每个时钟周期只能执行一条指令，因此它们的CPI至少为一。然而，超标量处理器通过并行地在多个执行单元上同时处理多条指令，可以实现更高的指令吞吐量。如果一个超标量处理器在一个时钟周期内平均执行多于一条指令，其CPI就会小于一。
这种能力取决于多种因素，包括处理器的设计、执行单元的数量、指令流中可用于并行执行的指令数量以及硬件如何处理数据冒险和控制冒险等因素。因此，虽然超标量处理器理论上可以实现CPI小于一，但实际的性能也受到程序特性和处理器设计的限制。

不熟悉的英语单词合集：

2022
copy-back protocol
Bit width
costlier

temporal
2021
spatial locality（空间局限性）

2020
subroutine 子程序
software oriented
bandwidth
latency
mechanism
compensate

2019
intermediates 中间体
property

2018
multithreading（多线程） and multicore（多核） rely on parallelism to get more efficiency from a chip（芯片）.